DIGITAL INDUSTRIES SOFTWARE

How Siemens EDA helps you **engineer smarter 5G communications systems faster**

Executive summary
The massive buildout for 5G communications is just getting underway, but its full economic impact – estimated to possibly reach $13.1T and provide 22.8 million jobs – is not expected to be fully realized until 2035. Siemens EDA and its parent, Siemens Digital Industries Software, with the Xcelerator portfolio – spanning from IC, packaging and PCB/systems electronic design, software design to mechanical design and manufacturing all the way to enterprise-level IC and system running in the field monitoring – are uniquely positioned to help companies deliver to market differentiated 5G-ready platforms and contend for the lion's share of this huge market.

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Introduction

In this paper, we first look at the promise of 5G communications and where it stands today. We then take a closer look at the 5G IC and systems design challenges and step through the IC and PCB solutions flows to show how Siemens EDA can help you engineer smarter 5G communications systems faster. Finally, we discuss how Siemens EDA solutions integrate with software, mechanical and PLM solutions in the Siemens Xcelerator portfolio. The Xcelerator portfolio enables companies and their suppliers to collaboratively build comprehensive digital twins using a model-based systems engineering methodology to deliver 5G and ultimately 6G systems to market faster.

Fulfilling the grand vision of 5G

Building on the previous four generations of wireless infrastructure that brought ever higher and more sophisticated levels of wireless communication and data transfer to the world, the grand vision for 5G communications is to bring everyone and everything together including machines, objects and devices. Leveraging artificial intelligence (AI) and machine learning (ML) at most points in the network, 5G will enable the buildout of smarter, connected everything – smart devices, smart businesses, smart factories, and sequentially higher levels of autonomous vehicles communicating with, or even guided by, smart cities and infrastructure. It's expected that when fully completed, 5G will accommodate one million devices per square kilometer and be so fast that remote surgery will become reality!

If you've watched the flurry of mobile phone and telecommunications company (telco) commercials promoting their 5G devices, networks and 5G subscription plans, you might get the impression that 5G is already here and is a done deal. But don't rush to schedule a surgeon across the globe to operate on you quite yet. In reality, today's versions of "5G networks" are largely a mix of early 5G technologies and older generation – 3G and 4G – infrastructure. The industry refers to these mixed networks as "non-standalone 5G (NSA 5G)." Today, there are a growing number of "spots" within these networks that use all 5G technologies – what the industry terms "stand-alone 5G (SA 5G)." But even today's SA 5G, while more advanced than 4G and NSA 5G, is still quite far from reaching 5G's grand vision of smart cities that guide autonomous vehicles safely through their streets or remote surgery, in which 5G and robotic surgical systems like Intuitive Surgical's Da Vinci enable a surgeon located in one city to perform surgery in real-time on a patient in another city across the globe.

Where 4G and today's version of SA 5G still operate in the 3kHz to 6GHz frequency range (referred to as FR1), 5G will eventually expand the frequency band range from 6GHz up to 300GHz. A segment within this range from 24GHz to 100GHz is designated for the commercial licensable spectrum. And within this range, a segment of the spectrum from 60-70GHz is designated for fixed wireless and mission-critical technologies, such as smart infrastructure and cities, remote surgeries, and industrial processes – all of which demand extreme performance and ultra-low latency of 1 to 3 milliseconds.

For 5G to reach its true potential, the industry needs to deploy technologies like Frequency Range 2's (FR2) mmWave and MassiveMIMO, which require the development of sophisticated high frequency, RF beamforming and related protocols. The mmWave and MassiveMIMO equipment will need to be deployed in massively greater numbers everywhere to enable the beamforming and line-of-sight operations that enable full coverage and the lowest latency.

The complexity of the technologies involved in making advanced 5G possible was certainly a driving factor behind the decision to base 5G on open standards (figure 1). Previous-generation networks were defined and created by only a few cellular operators worldwide, leaving telcos little choice but to purchase equipment (at a high premium) from one of these few manufacturers. For 5G, the telcos demanded that industry standards be used at all

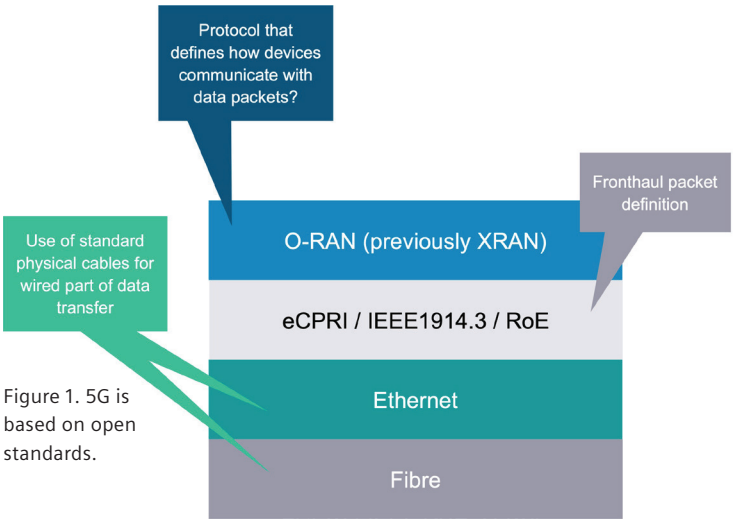

Figure 1. 5G is based on open standards.

layers of the network and that an open data packet protocol – what is called Open Radio Access Network (O-RAN) – be developed so that more companies could compete to develop ever-more advanced 5G network equipment. The competition will hopefully increase the pace of 5G innovation while, in the end, reducing the cost and increase the capabilities of the network. However, opening up 5G to greater competition means that verification and validation is imperative at every point in the network and holistically across electrical, software and mechanical domains before network deployment.

A key goal in developing differentiated advanced 5G systems is not just achieving the highest performance and lowest latency technologies but also achieving the highest performance per watt (PPW) for both the infrastructure equipment (front-haul and back-haul) and the edge devices (many of which are battery powered) connected to the 5G infrastructure while maintaining high reliability. The 3GPP and IMT-2020 have aggressive "watt per bit goals." These 5G organizations are calling for a 10x power reduction per bit.

Minimizing power per watt is important to accommodate the massive increase in 5G bandwidth. 5G is expected to consume an estimated 50 to 70 percent more power worldwide than 4G communications [1].

Huawei reports that each installation of its early 5G base stations consumes 11,577W, which is 68 percent more than its 4G base stations [2]. However, if looked at in terms of "watt per bit," 5G is indeed 10x more power-efficient than 4G. But it must be conceded that to be truly effective, 5G will require many more installations than 4G networks, so power consumption of the entire 5G network will be much higher than 4G. The 5G power signature could also be reduced further through the deployment of software-defined network SDN sleep modes that dynamically power down equipment when not in heavy use or in remote locations. Regardless, telcos will likely place a higher demand on systems that achieve the highest performance and lowest latency goals while keeping power as low as possible. Similarly, companies designing edge devices also seek optimal PPW – as their devices are often battery powered – and operational run time is a key selling point of many devices.

At the heart of the 5G wireless communications infrastructure and the many nodes/edge devices that will communicate through it, are sophisticated systems on chip (SoCs) that increasingly incorporate machine learning (ML) embedded processing engines to make 5G systems more efficient. Designing and verifying these SoCs and the systems they power can be a very complex process. They must be functionally correct but must also be validated and tested to work properly and optimally at the system and software levels and in many scenarios of operation in the context of the larger 5G infrastructure.

Let's look at the 5G IC design considerations as we walk through the entire IC design process from architectural design to silicon. We'll then look at the PCB design flow and scenarios where the closed-loop flow offered by the Siemens Xcelerator portfolio offers unmatched benefits for holistic 5G solutions development.

5G innovation starts with system IC architecture exploration

Whether it's designing 5G infrastructure or the many Internet of Thing (IoT) edge nodes/devices that connect to the network, developing an ideal IC architecture for 5G infrastructure and applications has many considerations and many routes to success.

FPGA – Design teams can use FPGA-based ICs for early, first-to-market deployment in 5G infrastructure, with the additional benefit of field programmability. The tradeoff is the higher power consumption and per-device costs with FPGA-based ICs and FPGA-SoCs. However, the benefits of being first to market with a product that can potentially be reconfigured to accommodate changing protocols and standards may easily mitigate the cost and power issues.

As has been the case in the past, after 5G protocols and standards have been established and the sockets secured, companies will migrate these 5G FPGA sockets to lower cost, lower power ASIC/SoC configurations. Simplifying the transfer of the design from a vendor-specific FPGA tool suite to a vendor-neutral, third-party tool, such as Siemens EDA's Precision™ RTL, enables teams to more readily target multiple FPGA vendor devices. Being able to use multiple vendors helps to optimize supply and cost issues and to more easily re-target designs to ASIC/SoC configurations down the line to improve profit margins.

High level synthesis, power analysis and FPGA-based prototyping – 5G is inherently an algorithm-heavy technology, as it calls for "new data flow algorithms to achieve better spectrum allocation, very high data rates, larger coverage areas, high-directional beamforming, less network leakage, and a higher overall system capacity [3]." Many of these algorithmic functions can be optimized if hardened and deeply integrated into the SoCs at the heart of 5G systems.

Siemens EDA's Catapult™ HLS is a powerful solution for 5G IC architectural exploration and overall system exploration. The tool enables system architects to develop computational algorithms in C++ code and then quickly iterate on what functionality would run best on software and what functions should be hardened as IC logic inside of an SoC. This hardware/software co-optimization produces optimal IC and system functionality and is especially handy for developing customized AI/ML co-processor blocks for 5G SoC applications. Developing your own AI/ML co-processor as opposed to using an off-the-shelf core can give your system a distinct PPW advantage and differentiation from competitors. One key example for 5G AI/ML is the complex channel estimation techniques that are required to optimize 5G Over-the-Air (OTA) communications channels.

FPGA vendors may have C-based HLS tools for their own programmable architectures, but Catapult is FPGA vendor-agnostic – it can be used for FPGA as well as SoC implementations, further assisting design teams in retargeting their hardware and software architectures to an ASIC implementation or another FPGA vendor's FPGA-based platform.

Catapult HLS has a companion power analysis tool called PowerPro™ that architects can use to ensure they are meeting power requirements early. The same tool can be used in subsequent steps of IC design and verification to ensure that the RTL version and gate-level version of the design is maintaining power goals set by the architects at the C-level.

Design for test – It is during the IC architecture planning phase that architects must decide what type of on-chip testing IP they would like to insert into their designs. Implementing design for test (DFT) blocks into the design enables post-silicon testing equipment to more easily identify problems with individual chips before they are released to market. Siemens' Tessent is a leader in DFT technologies for logic, memory and mixed signal devices as well as for yield enhancement.

Embedded analytics – A relatively new and very progressive option for IC architecture design is embedded analytics. This technology space, pioneered by Siemens EDA's Tessent group with Tessent MissionMode™ and strengthened greatly with many more Embedded Analytics technologies via Siemens' acquisition of UltraSoC (UK), enables architects to embed IP into their ICs to monitor and analyze a variety of characteristics – such as performance, power consumption, thermal analysis, reliability, and security – of the IC over its lifetime. Embedded Analytics IP not only collects and analyzes on-chip data but can formulate and implement a local response where necessary. This enables companies to monitor the device and even the 5G system it powers in the field to spot problems early, perform more accurate preventative maintenance, direct corrective action, or simply refine next-generation ICs and systems architectures from data gathered from the IC in the field. In other words, it enables companies and their partners to achieve a greater degree of digitalization by giving them a closed-loop design environment to produce smarter products faster. Embedded Analytics is a vital component of a Silicon Lifecycle Management solution that controls SoCs from design to fabrication to end-use in the field.

2.5D/3D IC – If design teams would like even greater functionality in one socket or would like to achieve differentiation through a mix of new and licensable silicon (implemented in different silicon process technologies), they can move beyond a monolithic SoC configuration and develop a silicon-in-package or more sophisticated 2.5D or 3D IC for their 5G applications.

A 2.5D/3D configuration enables companies to place monolithic ICs and a growing number of purpose-built "chiplets" side by side on a silicon interposer for 2.5D IC configuration or stack them on top of each other in a 3D configuration. This enables companies to more easily integrate different varieties of ICs – like digital logic, memory and high-speed analog I/O – into a single device (instead of further apart on a PCB) to achieve greater PPW and functionality while achieving a degree of isolation/shielding that would not be possible in a monolithic configuration. Siemens EDA offers the industry's most widely used 2.5D/3D solution, called the Innovator3D IC solution, which spans from architectural design to manufacturing and test.

Silicon photonics – For teams on the cutting edge of IC design, Siemens EDA is a pioneer in the emerging IC technology called silicon photonics, a technology that promises to take communications to higher levels of performance. Just now emerging from research into commercial use and driving a great deal of investment in the venture capital community [4], silicon photonics brings fiber optics directly onto layers of ICs, thereby forgoing the need for outboard IO that moves signals from fiber optic cable to copper. Among many applications, it is expected to be deployed initially in long-haul communications and datacenter applications to vastly speed data transfer and overall network performance. Siemens pioneered two technologies – LightSuite Photonic Compiler and L-Edit Photonics – that enable layout teams to integrate photonics into their SoC designs. Of course, the decision to boldly go in this direction is initially an architectural decision.

5G IC logic design and verification considerations

Logic design – Siemens EDA offers a complete solution for IC design, verification, and validation of digital front end (DFE), fronthaul 5G ICs and other digital blocks. The digital logic design and verification flow starts with Siemens EDA's Questa Advanced Verification portfolio and is capped off with the Veloce Strato hardware-assisted verification portfolio (figure 2). The Questa Design solution with code linting, debugging, checking as well as clock-domain and reset-domain crossing and signoff helps designers to develop a correct-by-construction register transfer level (RTL) code representation of their design.

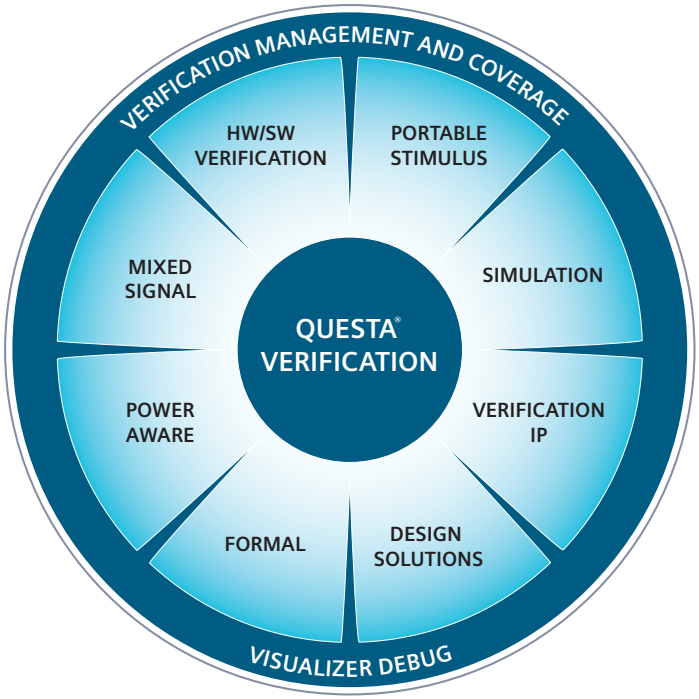

Figure 2. Questa Advanced Verification is complete verification solution for verifying 5G SoCs.

Logic verification and validation – The RTL code can then be run through Questa formal verification and dynamic simulation to find and then resolve issues at the block level. Design teams can then unite their RTL design blocks into a full-chip configuration in the Veloce Strato emulation system. This not only allows for full-chip functional verification of the RTL code but can also be used for validation of the IC design running in the context of the system. Veloce can be run in either in-circuit emulation (ICE) or virtual ICE modes, enabling engineering teams to connect to any available existing system hardware or functional models of hardware (a likely scenario in the emerging 5G space) to test firmware and application software running on the IC design. This allows teams to evaluate what needs to be changed in the IC design hardware and other hardware in the system in the context of a complete 5G-NR software stack before continuing to the next step in the IC design process.

Siemens EDA has a unique advantage in helping engineering teams design, verify and ultimately test their SoCs for 5G fronthaul IC and systems development. In 2018, Siemens acquired Sarokal Test Systems (Oulu, Finland) – a provider of a SoC test solutions for compliance with protocols into 5G fronthaul systems. From the stellar post-silicon test equipment that it gained in the acquisition, Siemens created a software-based application of the technology that verification teams can run inside of the Veloce Strato emulator for pre-silicon validation. These Siemens EDA VirtuaLAB apps provide representations/models of the fronthaul protocols. This

enables design teams to perform pre-silicon verification of interfaces running to and from SoCs being designed for O-RU (radio units) and O-DUs (distribution units). It also enables design teams to ensure their SoC designs are compliant and perform optimally before advancing the design to physical implementation and ultimately manufacturing the chip (figure 3).

During Veloce emulation, design teams can also use the new Veloce Hycon app to help offload known-good functions to a workstation to speed-up overall validation runtime.

When the RTL version of the chip design is verified and validated satisfactorily in Veloce Strato, the RTL can then be ported over to Veloce proFPGA or Veloce Primo FPGA-based prototyping solutions to give embedded and application software developers an early jump on software development – while the device is proceeding to physical design and verification – so the software can be ready when first silicon is delivered. Software designers can also use the emulator as a prototype system for early software development but porting to smaller prototyping systems allows more flexibility and a greater number of software engineers to work on a given project.

After the IC has been manufactured, hardware and software teams can then use the post-silicon test equipment, called Siemens Veloce X-STEP, to do

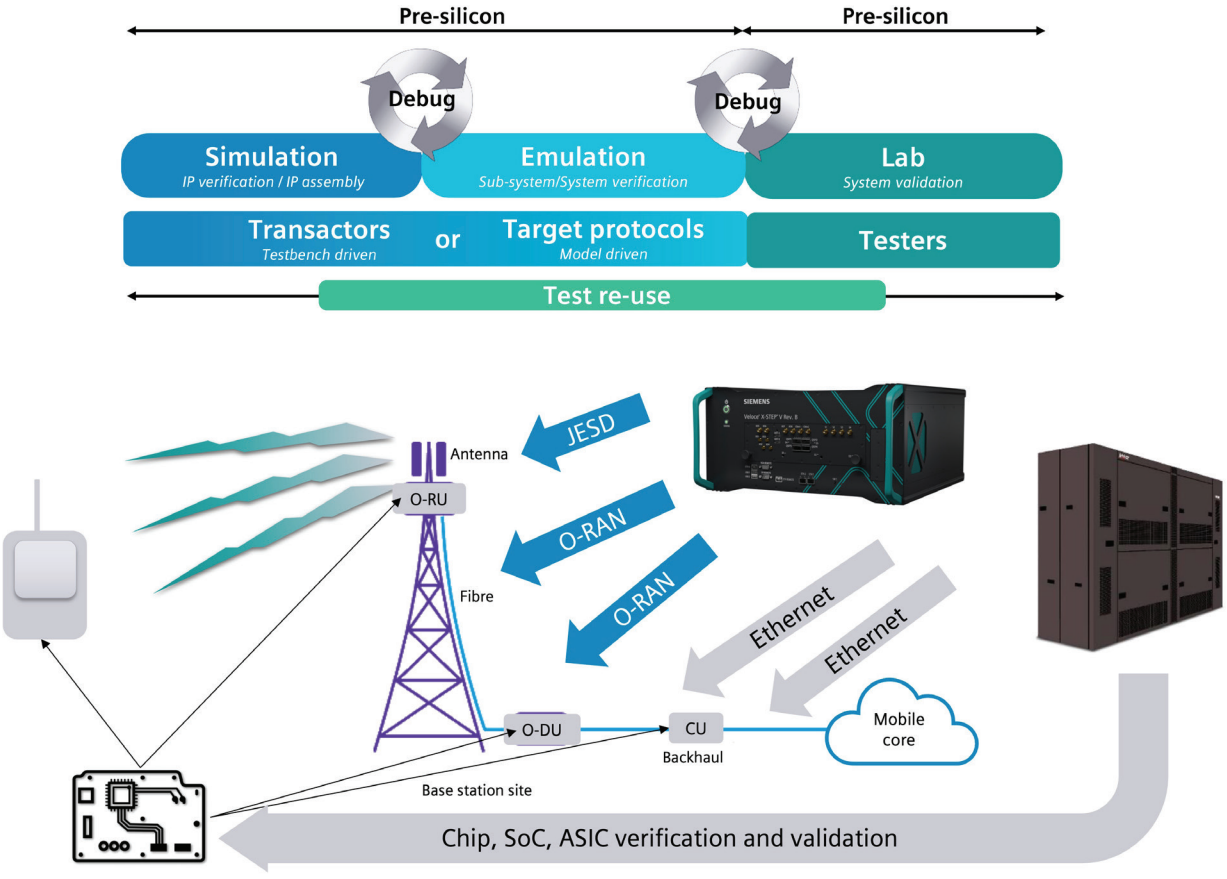

Figure 3. Siemens EDA is unique in that it's Veloce Strato emulation environment and Veloce X-STEP enable pre- as well as post-silicon validation of 5G protocols.

post-silicon validation. The protocol monitoring and generator (Protocol Generator and Protocol Analyzer) software inside the Veloce Strato emulator to validate the SoC design is identical to the software in the Veloce X-STEP hardware used for post-silicon validation – ensuring a closed-loop validation of compliance with protocols, JESD204B/C, CPRI, OBSAI, eCPRI, IEEE1914.3, RoE, and O-RAN. Veloce X-STEP can act as an O-RU or O-DU to enable thorough-unit testing and bit-accurate troubleshooting when O-RUs and O-DUs from different manufacturers are being integrated. As an active member of the various protocol committees, Siemens EDA updates protocols as soon as new versions become available.

Mixed-signal verification – Accurately verifying the links between the analog, high-frequency RF and digital domains is essential for SoC designs in 5G mobile/edge devices as well as 5G fronthaul equipment. Evermore advanced ADCs, DACs and clocking circuits are employed in many ICs/SoCs at various points of the 5G communications chain from inside handsets and edge devices to fronthaul antennae arrays. Siemens EDA's Symphony is a simulation vendor-agnostic, mixed-signal simulator that can help design teams simulate at the gate, Fast-SPICE and SPICE or levels any interface between digital and RF blocks (Verilog, SystemVerilog or VHDL) in an SoC, SiP or 3D IC design.

Library characterization – To ensure the libraries that the implementation/design tools will use to characterize a given IC design's building blocks (standard cells, memory and custom blocks) are silicon-process-accurate and robust for enough for 5G applications, Siemens EDA offers the Solido Characterization Suite.

Siemens EDA's Solido team pioneered the use of machine learning (ML) to derive accurate results faster. For example, Solido Generator uses ML methods to accelerate the overall library characterization process by instantly generating libraries for additional PVT corners after the initial characterization. Solido Generator uses existing SPICE-characterized libraries as anchor data to build ML models of the libraries and produce new PVT libraries.

Before generating the additional PVTs, Solido Generator analyzes the anchor corner set to determine the optimized set of libraries needed for additional PVT generation. Since the tool uses a set of pre-characterized .libs (timing libraries), it eliminates the dependency on SPICE netlists or subcircuits and the need to replicate characterization settings to match that of the library vendor. Solido Generator runs about 100 times faster than traditional SPICE. It generates production-accurate LVF .libs for additional PVT corners in a fraction of runtime it would take using Monte Carlo or approximated Monte Carlo methods, while retaining accuracy equivalent to its input anchor .libs.

The suite also includes Solido Analytics – an advanced library validation, analysis, and debugging solution that includes fast, parallelized, and comprehensive static rule-based checks, and employs an ML outlier detection tool that "learns" the expected characterized values in a library and automatically detects errors that typically go undetected with other tools.

5G IC physical design and verification considerations

Physical design – One of the fundamental demands of any 5G system, whether it be for 5G infrastructure or 5G edge devices, is to optimize for the best PPW. The SoCs designed for 5G infrastructure need to be extremely high-performance to receive, interpret and then transmit data as fast as possible. At the same time, 5G infrastructure equipment is estimated to consume anywhere from 50 to 68 percent more energy than 4G equipment. Telcos have an ongoing need to reduce energy footprints and related operating expenditures while still achieving performance requirements. In the physical implementation steps of SoC design, Siemens EDA now offers the Aprisa place and route solution, which uses the industry's most modern and advanced physical design technology to achieve optimal performance, power and area (PPA) for all applications.

With input from Siemens EDA's flexible mPower and third-party synthesis and timing engines, physical design teams can configure Aprisa to reach optimal levels of PPA faster and optimize designs for best performance per watt (PPW).

Custom digital and analog IC design – For teams developing high-speed I/O or any custom digital and analog chips and chiplets (for 3D IC) for 5G implementation, Siemens EDA offers the Tanner design solution. Tanner offers a complete custom/analog and MEMs flow from schematic capture to physical design and chip signoff with Siemens EDA's Calibre physical implementation solution to ensure your design is manufacturing ready and optimized for high yield.

Power integrity analysis – As a majority of 5G SoCs are a mix of digital, high-speed analog IO and mixed-signal IP blocks, 5G SoC design teams can use Siemens EDA's new revolutionary mPower power integrity solution to perform highly accurate EM/IR analysis across the entire IC. Where competing power integrity tools can only be used optimally for digital portions of an SoC, Siemens EDA's mPower solution is unique in the industry, as it is the only solution that can be used for digital, analog and mixed-signal designs.

Parasitic extraction – Because 5G ICs require a mix of leading-edge performance, low power and the highest degrees of reliability, design teams must create an accurate analog model of the parasitic effects of the structures and wires connecting those design elements – the complete circuit – so they can then perform exhaustive timing, power, circuit and signal integrity analysis of the design before moving it to Calibre signoff verification and manufacturing the device. Siemens EDA's Calibre xACT is an ideal solution for parasitic extraction of 5G ICs. It supports the most advanced foundry device models, including FinFET, and leading-edge process nodes with accurate, deterministic results, with results from simultaneous multi-corner extraction precisely matching single-corner results. It uses standard SVRF rule files to produce parasitic netlist formats and is interoperable with Calibre nmLVS circuit verification and Calibre nmDRC physical verification platforms.

Physical verification – Ensuring your 5G design will be manufacturable at your targeted foundry's silicon manufacturing process shouldn't be left to tools that are second or third best. Siemens EDA's Calibre design solutions portfolio is the proven signoff verification solution the IC design community has turned to for over two decades to ensure their IC designs are ready for manufacturing. Now offered with acceleration on-demand in cloud, fog as well as standard on-site configurations, Calibre allows design teams to signoff and get their designs to manufacturing even faster.

A new paradigm for 5G systems PCB collaboration and faster delivery

As the chipsets for 5G infrastructure advance in sophistication to move 5G infrastructure beyond 10GHz/cmWave configurations into configurations with mmWave and MassiveMIMO supporting beamforming, the complexity of the design of PCBs within these systems will also increase dramatically.

Design teams will need to implement 5G boards with an increasing number of layers to accommodate not only the routing of massive pin counts of these ICs, but also to isolate and shield high-speed digital traces from high-frequency RF circuitry to ensure overall system reliability. Signal integrity and power analysis will become a must-have at every step of the design process.

To support massiveMIMO with beamforming configurations, the sheer number of antennae array installations are expected to increase exponentially and be placed wherever possible in urban settings to enable beamforming/point-to-point communications. Further, the antennae arrays will come in all shapes and sizes, ranging from femtocells inside buildings to macrocells on towers to accommodate mass placement and space restrictions. They will all need to be tested not only for signal integrity but also thermal analysis to ensure they perform to specification while operating in a wide range of configurations, environments and use scenarios.

The teams that design printed circuit boards for 5G applications need a PCB systems design environment that can not only handle the complexity of connecting faster and potentially noisier devices in smaller form factors, they also need a design environment that is closely linked with customers, manufacturing and suppliers to ensure they can deliver complete product lines that meet customer specifications with the quality and volume of parts required.

Siemens EDA has an unmatched solution for companies developing 5G product lines. In terms of pure EDA technology, Siemens EDA offers complete PCB design environments with PADS Professional for small businesses and Xpedition Enterprise for medium to large enterprises. Siemens EDA's HyperLynx signal integrity solution works across both design environments to enable teams to perform comprehensive signal integrity throughout the design process. As part of the Xcelerator portfolio, Siemens also offers thermal simulation and analysis in SimCenter and the Valor PCB manufacturing solutions.

What's more, with Siemens' 2021 acquisition of Supplyframe – a digital marketplace for the global electronics value chain – Siemens is integrating seamless links to Supplyframe's network of manufacturers and part suppliers into the PADS Professional and Xpedition Enterprise environment. This will bring real-time supply chain information and collaboration technologies to PADS Pro and Xpedition directly users' desktops.

Offered as a Software as a Service (SaaS) add on to PADS Professional today and soon for Xpedition Enterprise, this enables design teams to work collaboratively on designs with other engineering teams, customers and manufacturing; receive real-time information on part availability and pricing from suppliers; and enables enterprises to find the best bids from manufacturing to increase profit margins.

Xcelerator offers an unmatched advantage for 5G ecosystem development

The Siemens Digital Industries Software is unique in the breadth of its Xcelerator portfolio. The ongoing conversion of technologies within the portfolio enables companies developing 5G systems to establish a closed-loop flow that links chip, IC package and PCB systems engineering efforts with electro-mechanical design, mechanical design with device unit testing, integration, troubleshooting and potentially even networks/ecosystem management – all together. Siemens Xcelerator enables companies to build a comprehensive digital twin implemented with a model-based systems engineering (MBSE) methodology to develop and test systems and ecosystems thoroughly in the virtual world before incurring the expense of manufacturing and deployment in the real world.

Take the example of fronthaul equipment of a 5G network. These units will be built in multiple configurations and form factors by multiple vendors to evolving design specifications and be deployed in a wide range of scenarios and environments. They will potentially be exposed to extreme cold, heat and sunlight and moisture, even vandalism (human and bird strikes) and vibrations. At the end of the day, they must be reliable, especially if they are to be employed for transmitting extreme low-latency, mission-critical data.

Assuming all components will be tested individually to meet tolerance specifications does not ensure that a system will meet specifications and reliability requirements once all the components are assembled and interacting. With a link between IC verification, IC package, software verification, PCB verification and mechanical verification, companies and their suppliers can more thoroughly verify their components running in the context of the entirety of their ecosystems/networks before deployment. What's more, with Tessent Embedded Analytics integrated into the heart of these systems at the IC level, both the chip and systems companies can monitor the health and security of their products even after the systems are deployed to spot and correct problems, better schedule preventative maintenance, and improve next-generation products faster.

With Siemens EDA as part of the Siemens Xcelerator, companies developing in the 5G and – soon to be 6G – market have a competitive advantage in engineering a smarter future faster...for us all.

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About Siemens Digital Industries Software

Siemens Digital Industries Software is driving transformation to enable a digital enterprise where engineering, manufacturing and electronics design meet tomorrow. Xcelerator, the comprehensive and integrated portfolio of software and services from Siemens Digital Industries Software, helps companies of all sizes create and leverage a comprehensive digital twin that provides organizations with new insights, opportunities and levels of automation to drive innovation. For more information on Siemens Digital Industries Software products and services, visit siemens.com/software or follow us on LinkedIn, Twitter, Facebook and Instagram. Siemens Digital Industries Software – Where today meets tomorrow.

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